

# AMTC04 DIGITAL ELECTRONICS

## UNIT-1 NUMBER SYSTEMS AND CODES

- 1.1 Binary Number System, Octal Number System, Hexadecimal Number System, Bits and Bytes, 1's and 2's Complements,
- 1.2 Decimal-to-Binary Conversion, Decimal-to-Octal Conversion,
- 1.3 Decimal-to-Hexadecimal Conversion, Binary-octal and Octal-Binary Conversions, Hexadecimal-Binary and Binary-Hexadecimal Conversion,
- 1.4 Hexadecimal-Octal and Octal-Hexadecimal Conversion.
- 1.5 BCD Code, Excess-3 Code, Gray code, Alphanumeric Codes, Parity Bits, Hamming Code, Floating Point Numbers.

## UNIT-2 BINARY ARITHMETIC

- 2.1 Basic Rules of Binary, Addition of Larger Bit Binary Numbers, Subtraction of Larger Bit Binary Numbers, Addition Using 2's Complement Method, Subtraction Using 2's Complement Method,
- 2.2 Binary Multiplicity-repeated Left Shift and Add Algorithm, Binary Division-Repeated Right Shift and Subtract Algorithm.

## UNIT-3 LOGIC GATES AND LOGIC FAMILIES

- 3.1 Positive and Negative Logic, Truth Tables, Logic Gates, Fan out of Logic Gates, Logic Families, TTL Logic Family,
- 3.2 CMOS Logic Family, ECL Logic Family, NMOS AND PMOS Logic Families.

## UNIT-4 BOOLEAN ALGEBRA AND MINIMISATION TECHNIQUES

- 4.1 Boolean Algebra vs Ordinary Algebra , Boolean Expressions- Variables and Literals, Boolean Expressions-Equivalent and Complement,
- 4.2 Theorems of Boolem Algebra, Minimization Techniques ,Sum-of-products Boolean Expressions,
- 4.3 Quine- McCluskey Tabular Method, Karnaugh Map Method, Karnaught Maps for Boolean Expressions: With More Than Four Variables.

## UNIT-5 COMBINATIONAL LOGIC CIRCUITS

- 5.1 Combinational Circuits, Implementation Combinational Logic, Arithmetic Circuits –Basic Building Blocks, Adder- Subtracted, BCD Adder,
- 5.2 Carry Propagation- Look Ahead Carry Generator, Arithmetic Logic Unit (ALU), Multitpliers, Magnitude Comparator, Parity Generator and Checker,
- 5.3 De-multiplexers and Decoders, Encoders, Read Only Memory (ROM), Programmable Logic Array (PLA)

## UNIT-6 FLIP FLOPS AND RELATED DEVICES

- 4.1 R-S Flip Flop, Level Triggered and Edge Triggered Flip Flops, J.K Flip Flop,
- 4.2 Master-slave Flip Flops, T-flip Flop, D flip Flop, Synchronous and Asynchronous Inputs.

## **UNIT-7 COUNTERS AND REGISTERS**

- 7.1 Ripple Counter vs. Synchronous Counter, Modulus (or Mod-Number)of a Counter, Propagation Delay in Ripple Counters, Binary Ripple Counters- Operational Principle,
- 7.2 Binary Ripple Counters with Modulus Less Than ( $2^n$ ), Synchronous (or Parallel ) Counters, Up/Down Counters, Decade and BCD Counters , Presetable Counters, Shift Register,
- 7.3 Serial-in Serial-out Shift Register, Serial-in Parallel-out Shift Register, Parallel-in, Serial-out Shift Register, Parallel-in, Parallel-out Shift Register, Shift Register Counters- Ring Counter, Shift Counter.

## **UNIT-8 SEMI-CONDUCTOR MEMORY**

- 8.1 RAM Architecture,
- 8.2 Static RAM (SRAM),
- 8.3 Dynamic RAM (DRAM),

### **Reference Book:**

1. Digital and Analog Communication, Publisher Katsons, Writer Brijesh Verma

