# AMHE22 ADVANCED COMPUTER ARCHITECTURE

**UNIT-1 PARALLEL COMPUTER MODEL**

1.1 The State of Computing: Computer Development Milestones, Elements of Modern Computers, Evolution of Computer Architecture, System Attributes to Performance

1.2 Multiprocessors and Multicomputer: Shared-Memory Multiprocessors, Distributed memory Multicomputer, Taxonomy of MIMD Computers

1.3 Multisector and SIMD Computers: vector Supercomputers, SIMD Supercomputers

1.4 PRAM and VLSI Models: Parallel Random-Access Machines, VLSI Complexity Models

1.5 Architectural Development Tracks: Multiple-Processor Tracks, Multi vector and SIMD Tracks, Multithreaded and Dataflow Tracks

**UNIT-2 PRINCIPLES OF SCALABLE PERFORMANCE**

2.1 Performance Metrics and Measures: Parallelism Profile in Programs, Harmonic Mean Performance, Efficiency, Utilization and Quality, standard Performance Measures

2.2 Parallel Processing Applications: Massive Parallelism for Grand Challenges, Application Models of Parallel Computers, Scalability of Parallel algorithms

2.3 Speedup Performance Laws: Amdahl's Law for a fixed Workload, Gustafson's Law for scaled Problems, Memory-Bounded speedup Model

2.4 Scalability analysis and Approaches: Scalability Metrics and goals, evolution of Scalable computers

**UNIT-3 PROCESSORS AND MEMORY HIERARCHY**

3.1 Advanced Processor Technology: Design Space of Processors, Instruction-set architectures, CISC Scalar Processors, RISC scalar Processors

3.2 Superscalar and Vector Processors: Superscalar Processors, The VLIW Architecture, Vector and Symbolic Processors

**UNIT-4 BUS, CACHE, AND SHARED MEMORY**

4.1 Backplane Bus Systems: Backplane Bus Specification, Addressing and Timing Protocols, Arbitration, Transaction, and Interrupt, The IEEE Futurebus+ Standards

4.2 Cache Memory Organizations: Cache Addressing Models, direct Mapping and associative caches, set-associative and Sector caches, cache Performance Issues

4.3 Shared-Memory Organizations: Interleaved Memory Organization, Bandwidth and Fault tolerance, Memory allocation schemes

4.4 Sequential and weak consistency Models: atomicity and Event ordering, Sequential Consistency Model, Weak Consistency Models

**UNIT-5 PIPELINING AND SUPERSCALAR TECHNIQUES**

5.1 Linear Pipeline Processors: asynchronous and synchronous Models, Clocking and timing control, Speedup, efficiency, and throughput

5.2 Nonlinear Pipeline Processors: reservation and Latency analysis, Collision-free Scheduling, Pipeline Schedule Optimization

5.3 Instruction Pipeline Design: Instruction Execution Phases, Mechanisms for Instruction Pipelining, Dynamic Instruction scheduling, Branch handling techniques

5.4 Arithmetic Pipeline Design: Computer arithmetic Principles, Static Arithmetic Pipelines, Multifunctional Arithmetic Pipelines

5.5 Superscalar and Super pipeline Design: Superscalar Pipeline Design, Superpipelined Design, Supersymmetry and design Tradeoffs

**UNIT-6 MULTIPROCESSORS AND MULTICOMPUTERS**

6.1 Multiprocessors system Interconnects: Hierarchical Bus Systems, Crossbar Switch and Multiport Memory, Multistage and Combining Networks

6.2 Cache Coherence and Synchronization Mechanisms: The cache Coherence Problem, Snoopy Bus Protocols, Directory-Based Protocols, Hardware Synchronization Mechanisms

6.3 Three Generations of Multicomputers: design Choices in the Past, Present and Future Development, The Intel Paragon System, Deadlock and virtual Channels, Flow Control Strategies, Multicast Routing Algorithms

**Reference Books:**


1. Nicolas P Carter, Computer Architecture and Organization, Tata McGraw Hill, 2nd Edition.
2. D. Sima, T Fountain and P Kacsuk, Advanced Computer Architecture: A Design space approach, Pearson education, 2000.