AMET-18: MICRO PROCESSOR

1. MICROPROCESSOR ARCHITECTURE AND MICROCOMPUTER SYSTEM

Objectives, the microprocessor is a programmable logic device, designed with registers, flip-flops, and timing elements, memory, r/wm (read/write memory), rom (read-only memory), ee-prom (electrically erasable prom), recent advances in memory technology, input and output (i/o) devices, example of a microcomputer system, review: logic devices for interfacing, examples of latches.

2. 8086 MICROPROCESSOR ARCHITECTURE AND MEMORY INTER-FACING

Objectives, the 8085 mpu, address bus, multiplexed address/data bus, control and status signals, power supply and clock frequency, externally initiated signals, serial i/o ports, the alu, timing and control unit, instruction register and decoder, register array, example of an bobs-based microcomputer, memory interfacing, the sdk-85 memory system', how does an 8085-based single-board microcomputer work?

3. INTERFACING I/O DEVICES

Objectives, basic interfacing concepts, out instruction (8085), in instruction, interfacing output displays, circuit analysis, program, program description, problem statement, hardware description, seven-segment led, interfacing circuit and its analysis, interfacing input devices, memory-mapped i/o, execution of memory-related data transfer instructions, output port and its address, input port and its address, testing and troubleshooting i/o interfacing circuits, some questions and answers.

4. INTERRUPTS

objectives, the 8085 interrupt, rst (restart) instructions, problem statement, main program, description of the interrupt process, testing interrupt on a single-board computer system, issues in implementing interrupts, 8085 vectored interrupts, trap, rst 7.5, 6.5, and 5.5, triggering levels, pending interrupts, problem statement, hardware description, monitor programe, main program, program description, internet service routine, restart as software instructions, problem statement, problem analysis, breakpoint subroutine, program discription, additional i/o concepts and processes, 8259a interrupt operation.

5. INTERFACING DATA CONVERTERS

Objective, digital-to-analog (d/a) converters, r/2r ladder network, problem statement, hardware description, program, operating the d/a converter in a bipolar range, hardware description, analog-to-digital (aid) converters, interfacing an 8-bit a/d converter using status check, hardware description, interfacing circuit, service routine, dual-slope a/d converters.

6. SDK-85 PROGRAMMABLE INTERFACE DEVICES

Objective, basic concepts in programmable devices, data input with handshake, data output with handshake, the 8155/8156 and 8355/8755 multipurpose programmable devices, control logic, the 8155 i/o ports, chip enable logic and port addresses, control word, hardware description, control word, program description, problem statement, control signals in

handshake mode, input, output, status word, problem statement, problem analysis, port addresses, program description, interrupt i/o, the 8279 programmable keyboard/displa y interface, keyboard section, scan section, display section, mpu interface section, circuit description, decoding logic and port addresses, initialization instructions.

7. GENERAL-PURPOSE PROGRAMMABLE PERIPHERAL DEVICE

Objective, the 8255a programmable peripheral interface, control logic, bsr control word, port address, subroutine, problem statement, problem analysis, mode 0: control word, bsr control word for start pulse, subroutine, program description, mode 1: input control signals, control and status words, programming the 8255a in mode 1, mode 1: output control signals, control and status words, problem statement, program description, illustration: interfacing keyboard and seven-segment display, key debounce, illustration : bidirectional data transfer between two microcomputers, data transfer from master mpu to slave mpu, data transfer from slave to master mpu, control word-mode 2, status word-mode 2, read and write operations of the slave mpu, program comments, slave program, The 8254 (8253) Programmable Interval Timer, Data Bus Buffer, Control Logic, Mode, Write Operations, Read Operations, Problem Statement, Mode 0: Interrupt On Terminal Count, Mode 1: Hardw Are-Retriggerable One-Shot, Mode 2: Rate Generator, Mode 3: Square-Wave Generator, Mode 4: Software-Triggered Strobe, Mode 5: Hardware-Triggered Strobe, Read-Back Command, The 8259a Programmable Interrupt Controller, Read/Write Logic, Control Logic, Interrupt Registers And Priority Resolver, Cascade Buffer/Comparator, End Of Interrupt, Additional Pea Tures Of The 8259a, Direct Memory Access (Dma) And The 8257 Dma Controller, Dma.Channels, Need For 8212 And Signal Adstb, Signal Aen (Address Enable), Initialization, Dma Execution.

8. SERIAL I/O AND DATA COMMUNICATION

Objectives, Basic concepts in serial i/o, Synchronous vs, Asynchronous transmission, Simplex and duplex transmission, Rate of transmission (baud), Parity check, Checksum, Cyclic redundancy check (crc), Software-controlled asynchronous serial i/o, Serial output data (sod), Serial input data (sid), Hardware-controlled serial i/o using programmable chips, Read/write control logic and registers, Transmitter section, Receiver section, Initializing the 8251a, Program description.

9. MICROPROCESSOR APPLICATION

Objectives, Designing scanned displays, Sn 75491-segment driver, Sn 75492-digit driver, Interfacing a matrix keyboard, Keyboard subroutine, Mm74c923 keyboard encoder, Memory design, Eprom memory, Wait state calculations, 8086 mpu design, Address bus, Data bus, Control signals, Frequency and power requirements, Externally triggered signals, Designing a system: single-board microcomputer, Keyboard, Display, Execute, System buses and their driving capacity, Keyboard and displays, Software design, Program coding, Development and troubleshooting tools, Emulation process, Features of in-circuit emulator, Debugging tools.

10. INTRODUCTION TO 8085 ASSEMBLY LANGUAGE PROGRAMMING

Objectives, the 8085 programming model, registers, accumulator, flags, program counter (pc), stack pointer (sp), instruction classification, data transfer (copy) operations, arithmetic operations, logical operations, branching operations, machine control operations, instruction format, one-byte instructions, two-byte instructions, three-byte instructions